# EXHIBIT 3

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Paper 6
Entered: March 13, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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CISCO SYSTEMS, INC.,
Petitioner,

v.

LIONRA TECHNOLOGIES, LTD.,
Patent Owner.

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IPR2024-01281
Patent 7,738,471 B2

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Before WILLIAM V. SAINDON, THOMAS L. GIANNETTI, and RUSSELL E. CASS, *Administrative Patent Judges*.

SAINDON, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
*35 U.S.C. § 314*

# I. INTRODUCTION

## *A. Background and Summary*

Cisco Systems, Inc. ("Petitioner") filed a Petition (Paper 2, "Pet.") requesting an *inter partes* review of claims 1–3, 5–10, 12–15, and 17–21 ("the challenged claims") of U.S. Patent No. 7,738,471 B2 (Ex. 1001, "the '471 patent"). Lionra Technologies, Ltd. ("Patent Owner") did not file a preliminary response.

We have authority to determine whether to institute an *inter partes* review under 35 U.S.C. § 314(b) and 37 C.F.R. § 42.4(a). The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted unless "there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." For the reasons provided below, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing with respect to at least one challenged claim of the '471 patent, and we institute an *inter partes* review. 37 C.F.R. § 42.108(a).

Our findings of fact, conclusions of law, and reasoning discussed below are made for the sole purpose of determining whether the Petition meets the threshold for initiating review. This decision to institute trial is not a final decision as to the patentability of any challenged claim or the construction of any claim limitation.

## *B. Real Parties in Interest*

The parties both assert that they are the sole real parties in interest. Pet. 72; Paper 4, 2 (Patent Owner's Mandatory Notice).

### C. *Related Matters*

The parties both identify *Lionra Technologies Ltd. v. Cisco Systems, Inc.*, No. 2:24-cv-00097 (E.D. Tex.), as a related matter outside the USPTO. Pet. 72; Paper 4, 2.

### D. *Prior Art and Asserted Grounds*

Petitioner's grounds rely on the following prior art references:

| Name | Reference | Exhibit No. |
|---|---|---|
| Russell | US Pat. 6,678,746 B1, iss. Jan. 13, 2004 | 1025 |
| Nelson | US Pat. 7,333,489 B1, iss. Feb. 19, 2008 | 1006 |
| Cornett | US Pub. 2006/0072564 A1, pub. Apr. 6, 2006 | 1005 |
| Paatela | US Pub. 2006/0209840 A1, pub. Sept. 21, 2006 | 1007 |

Petitioner asserts that the challenged claims would have been unpatentable on the following grounds:

| Claim(s) Challenged | 35 U.S.C. § | Reference(s)/Basis |
|---|---|---|
| 1–3, 5–10, 12–15, 17–21 | 103 | Cornett, Paatela, Nelson |
| 8 | 103 | Cornett, Paatela, Nelson, Russell |

Petitioner relies on the testimony of Nader Mir, Ph.D., a professor of Electrical Engineering who testifies he performs research and teaches courses in "computer networks, networking devices, switches, routers, virtualization, virtual switches, cloud computing, software-defined networking in clouds, and cloud data centers." Ex. 1003 ¶ 10.

### E. *Overview of the '471 Patent*

The '471 patent is directed to high-speed protocol header processing at a node of a packet-based communications network. Ex. 1001, 1:9–11. In a packet-based communications network (e.g., TCP/IP), payload data, such as video data, is encapsulated in a series of protocol stack headers. *Id.* at

1:13–25. Each of the different layers is responsible for handling a different aspect of communication between the nodes in the network. *See id.* at 1:40–65; Ex. 1003 ¶¶ 26–32 (describing various known layer models).

The '471 patent notes that processing the various headers can lead to relatively long delays. Ex. 1001, 1:64–65. According to the '471 patent, in a conventional system, each of the protocol stack layers has its header written to the packet buffer memory after the packet is received (*id.* at 5:51–54), and then the information in each header is processed in a sequential manner (*id.* at 10:47–48). *See also id.* Fig. 5 (depicting an example prior art configuration). The '471 patent proposes to instead concurrently write the specific layer header fields directly into both the packet buffer memory (as in the conventional system), as well as a space specifically set aside for each protocol stack layer. *Id.* at 5:64–6:1, Fig. 4. According to the '471 patent, doing so "allow[s] each of the protocol stack layers to concurrently begin header processing without having to wait for one or more other protocol stack layer[]s to complete its header processing." *Id.* at 6:24–28.

### *F. Challenged Claims*

Claims 1–3, 5–10, 12–15, and 17–21 are challenged. Claims 1 and 13 are independent. Claim 13 is reproduced below.

> 13. An egress end user node (EEUN) of a packet based communications system, comprising:
>
> a decoder configured for decoding a packet having a plurality of headers; and
>
> a direct memory access (DMA) device coupled to said decoder and configured for concurrently writing (1) each of said plurality of headers to a packet buffer memory and (2) each individual one of said plurality of headers to a respective protocol

stack layer memory where it is available for immediate processing within a protocol stack layer.

## II. ANALYSIS

### *A. Legal Standards Used in the Merits Analysis*

"In an IPR, the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim")); *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (discussing the burden of proof in *inter partes* review).

A claim is unpatentable under 35 U.S.C. § 103 if "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious . . . to a person having ordinary skill in the art to which said subject matter pertains." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) when in evidence, objective indicia of non-obviousness. *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17–18 (1966).

### *B. Level of Ordinary Skill in the Art*

Petitioner asserts that:

> A Person of Ordinary Skill in The Art ("POSITA") in Sept. 2007 would have had a working knowledge of network communications techniques and highspeed packet processing technologies. Ex.1003, ¶20. A POSITA would have had a bachelor's degree in computer science, computer engineering, electrical engineering, or an equivalent training, and approximately two years of work experience in network communications. Lack of work experience can be remedied by additional education, and vice versa. Ex.1003, ¶20.

Pet. 13. We use this definition for purposes of this Decision because it appears consistent with the level of skill reflected in the prior art and the '471 patent.

### *C. Claim Construction*

Under 37 C.F.R. § 42.100(b), we apply the claim construction standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc). That is, "the words of a claim 'are generally given their ordinary and customary meaning' . . . that the term would have to a person of ordinary skill in the art in question at the time of the invention." *Id.* at 1312–13.

Petitioner asserts that no terms require express construction. Pet. 13. We do not expressly construe any terms at this time. *Realtime, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) ("The Board is required to construe 'only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.'") (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

*D. Asserted Obviousness Over Cornett, Paatela, and Nelson (Claims 1–3, 5–10, 12–15, and 17–21)*

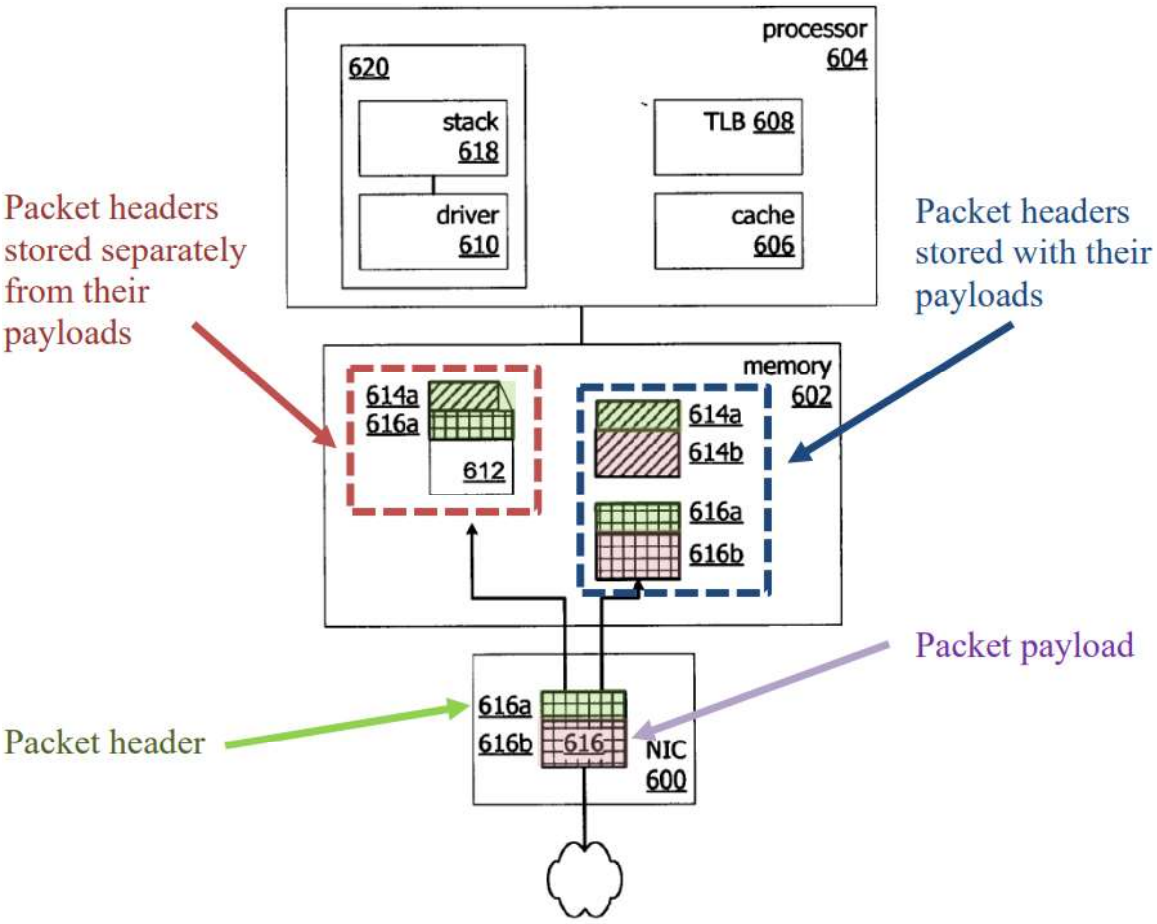
Patent Owner did not file a preliminary response. The only question before us at this time is whether Petitioner has established a reasonable likelihood of success for at least one claim. We analyze independent claim 13.

At a high level, independent claim 13 is directed to an egress end user node of a packet-based communications system. The node has a decoder and a direct memory access device. The direct memory access device is configured for concurrently writing a plurality of packet headers to (i) a packet buffer memory and (ii) a protocol stack layer memory. According to the '471 patent, the protocol stack layer memory separately stores each layer of the protocol stack, so that they can be accessed and processed concurrently. Ex. 1001, 5:54–56, 6:22–31, Fig. 4 (items 126, 128, 130, 132, 134).

Petitioner asserts that the network interface card of Cornett is the claimed egress end user node. Pet. 32–33. Petitioner asserts that Cornett's network interface card includes a physical layer device that "translates between the analog signals of a communications medium . . . and digital bits." *Id.* at 33 (quoting Ex. 1005 ¶ 79). According to Petitioner, the physical layer device is configured for decoding a packet and, thus, is the claimed decoder. *Id.* at 33–34. Petitioner also points out that Cornett's network interface card "can cause storage 704 (e.g., via Direct Memory Access (DMA)) of the packet's header" in memory. *Id.* at 34–35 (quoting Ex. 1005 ¶ 74). According to Petitioner, the direct memory access engine in Cornett is the claimed direct memory access device. *Id.*; Ex. 1005 ¶ 97

("TCP/IP processing may be accelerated by using a data movement module, such as a DMA engine, to move data from one buffer to another buffer.").

Claim 13 then requires the direct memory access device to be configured for concurrently writing a plurality of packet headers to two locations. Petitioner asserts that Cornett depicts writing a plurality of packet headers to two locations in Figure 10. Below is a reproduction of Petitioner's annotated Figure 10 of Cornett.



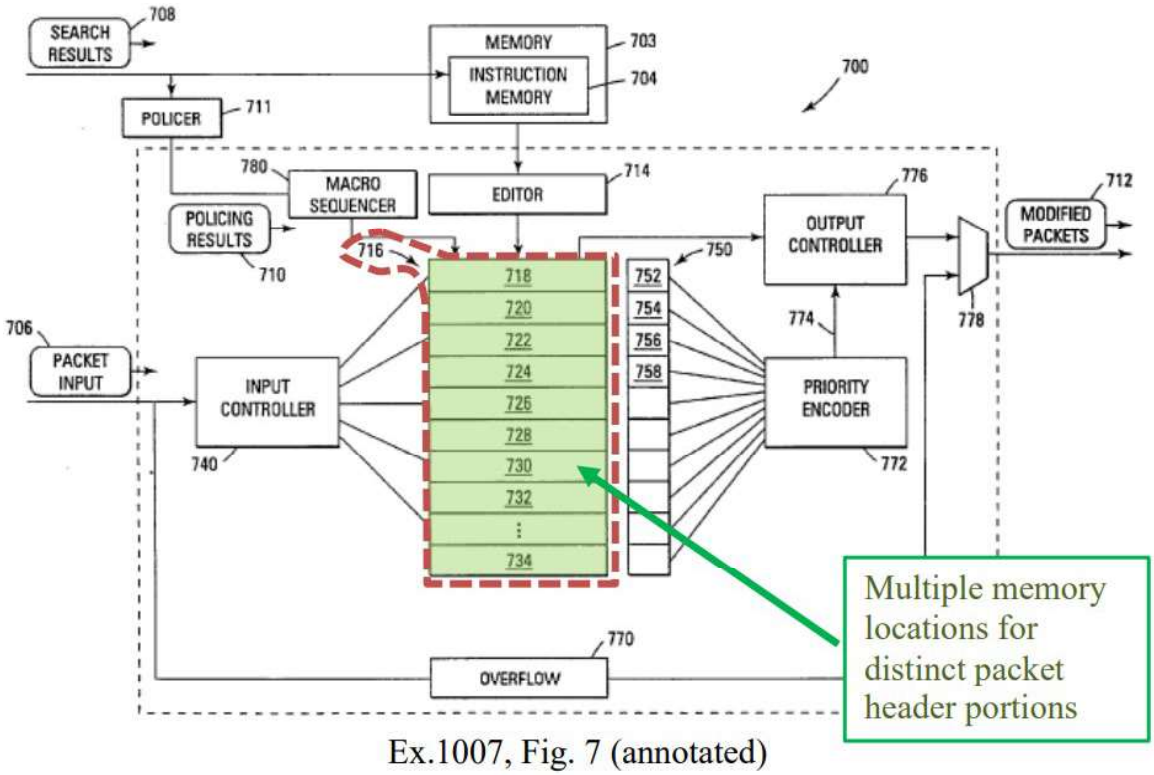

Ex.1005, Fig. 10 (annotated)

Pet. 37. Starting at the bottom, Petitioner's annotated version of Figure 10 of Cornett depicts network interface card (NIC) 600 connected to a network (shown as a cloud). Ex. 1005 ¶ 68. Network interface card 600 receives packet 616, made of packet header 616a (green) and packet payload 616b

(purple). *Id.*; *id.* ¶ 69. This information is then stored in memory 602. *Id.* In page 612 of memory 602 (red dashed box denoted by Petitioner as "Packet headers stored separately from their payloads"), packet header 616a is stored alongside the header of an earlier-received packet, 614a, both without their corresponding payloads. *Id.* ¶ 81. The purpose of storing packet headers only in page 612 is so that they can be more quickly accessed and processed. *Id.* ¶ 64. The entirety of packets 614 and 616 are stored in a separate buffer location in memory 602 (blue dashed box denoted by Petitioner as "Packet headers stored with their payloads"). *Id.*

Petitioner asserts that the location in memory 602 of Cornett that stores the entire packet (blue dashed box) is the claimed "*packet buffer memory*." Pet. 37; *see also id.* at 36–38 (entire argument).

As to the claimed "protocol stack layer memory," Petitioner asserts that Cornett does not describe in detail how page 612 in memory 602, which stores just the headers (red dashed box), operates. *Id.* at 38. Petitioner therefore directs our attention to Paatela, which stores "packet portions correspond[ing] to headers of the various protocol layers associated with the incoming packet." *Id.* at 39 (quoting Ex. 1007 ¶ 77); *see also id.* at 39–41 (entire argument). Figure 7 of Paatela, annotated by Petitioner, is reproduced below.




Ex.1007, Fig. 7 (annotated)

Pet. 40. Figure 7 of Paatela shows memory 716, which "is partitioned such that at least some of these segments [718–734] are allocated to store data corresponding to certain portions of the packets 706." Ex. 1007 ¶ 77. Paatela states, "these packet portions correspond to headers of the various protocol layers associated with the incoming packet." *Id.* Paatela explains that separately storing the packet headers makes it so that "editing of packet layer headers can be effectively and efficiently performed." *Id.* ¶ 79.

According to Petitioner, "[e]ach one of these segments of memory [in Paatela] corresponds to a *respective protocol stack layer memory* because each segment stores an individual layer packet header." Pet. 40 (citing Ex. 1003 ¶ 85). Petitioner asserts that the combination of Cornett and Paatela would have been "the use of known techniques . . . to improve a similar process . . . in the same way to yield predictable results." *Id.* at 25 (citing Ex. 1003 ¶ 57). Petitioner also asserts that Paatela supplements Cornett's

teachings by providing missing implementation details. *Id.* at 25–26 (citing Ex. 1003 ¶ 58), 40–41 (citing Ex. 1003 ¶ 86).

As to the claim requirement that the direct memory access device concurrently write the packet buffer memory and the protocol stack layer memory, Petitioner asserts that neither Cornett nor Paatela explicitly describes the timing of packet writing. Pet. 42. Petitioner asserts, however, that Nelson discloses writing a packet header separately and in parallel with writing the entire packet. *Id.* (citing Ex. 1006, 6:66–7:4; Ex. 1003 ¶ 89). Indeed, Nelson explains that the parallel storage action "avoid[s] having to read the frames out of the [larger frame] buffer" when reading a header, which eliminates the need for a separate reading step and "allows the routing decision to be made before the [frame] buffer becomes available." Ex. 1006, 2:1–22 (containing the quoted language), 7:1–4 (describing "parallel . . . storage"). Petitioner asserts that it would have been obvious to write the packet header at the same time as writing the entire packet in Cornett, because Cornett, Paatela, and Nelson are concerned with speed, and writing in parallel would increase speed (vs. writing serially). *Id.* at 43–44 (citing Ex. 1003 ¶ 90); *see also id.* at 26 (similar argument).

Reviewing Petitioner's position with respect to independent claim 13, we determine that Petitioner has addressed each limitation in sufficient detail and with adequate citations to the record. Petitioner has also provided sufficient reasons for combining the teachings of Cornett, Paatela, and Nelson with a reasonable expectation of success. Reviewing the record before us, we determine that Petitioner has established a reasonable likelihood of success in showing that claim 13 would have been obvious in view of Cornett, Paatela, and Nelson.

### *E. Remaining Claims and Grounds*

Absent dispute, and having already determined that Petitioner has met the threshold for institution, we do not review the remaining claims and grounds at this time.

## III. CONCLUSION

For the reasons given above, we determine that Petitioner has established a reasonable likelihood of success in showing that at least one claim of the '471 patent would have been obvious in view of the prior art cited. Accordingly, we institute *inter partes* review of all claims and grounds raised in the Petition. 37 C.F.R. § 42.108(a).

## IV. ORDER

In consideration of the foregoing, it is hereby

ORDERED that the Petition requesting *inter partes* review of claims 1–3, 5–10, 12–15, and 17–21 of the '471 patent is *granted*; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(a), *inter partes* review of the '471 patent commences on the entry date of this Decision, and pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial.

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